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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,596	09/12/2001	Anton Gunzinger	FREI P033US-2	8857

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EXAMINER
ELLIS, RICHARD L

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)	
09/954,596	Gunzinger, Anton	
Examiner	Group Art Unit	
Richard Ellis	2183	

--The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address--

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (Three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) Months from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on November 24, 2002.

☒ This action is FINAL

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 16-32. is/are pending in the application.

☐ Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 16-32. is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119(a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3.

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other _____

Office Action Summary

1. Claims 16-25 remain for examination. Claims 26-30 are newly presented for examination.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. Claims 16-20 are rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A) The scope of meaning of the following terms are unclear:

1. "each communications manager comprising predefined values" claims 16 and 21. It is unclear how a piece of hardware, i.e., the "communications manager" can comprise (i.e., be made up on, be created from) "predefined values". A communications manager can contain or can be assigned a predefined value, but it can not itself be "comprised" of those predefined values.

This rejection is maintained because applicant neither amended the claim to overcome it, nor presented any arguments as to why the rejection was improper.

4. Claims 16-25 are rejected under 35 USC 102(b) as being clearly anticipated by Brantley, Jr. et al., U.S. Patent 4,980,822.

Brantley, Jr. et al. taught (e.g. see figs. 1-8) the invention as claimed (as per claim 16), including a data processing ("DP") system comprising:

A) a method of operating a parallel computer system (fig. 1) having at least first and second processor elements (20), each processor element comprising a processor (fig. 2, 22), a local program memory (26, 30), a local data memory (26, 30), a communications manager (24, 28), and an operating system (inherent), within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus (fig. 8); the communications managers of the at least first and second processor elements communicative coupled by means of a message-passing communications network (fig.

1, 10); the processor elements each executing an application (inherent); each communications manager further having a plurality of predefined values indicative of global addresses in which the application of the processor element is interested (fig. 7, 258); the method comprising the steps of;

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B) writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element (col. 4 lines 56-60);

C) adding, by the communications manager, a global address to the result of the computation (fig. 7, "NODE #");

D) propagating, on the message-passing communications network (fig. 1, 10), a message comprising the global address and the result of the computation (col. 8 lines 36-39, lines 47-68, col. 9 lines 31-37 and 55-60);

E) receiving the message, via the message-passing communications network (fig. 1, 10), by the communications manager of the second processor element (col. 9 lines 45-54);

F) comparing, by the communications manager of the second processor element, the global address with the plurality of predefined values for a match (col. 9 lines 22-25, 45-54); and,

G) in the event of a match, computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory (col. 9 lines 45-49 , 51-54, and 65-68).

5. As to claim 17, Brantley, Jr. et al. taught that the predefined values were further characterized as comprising an address window, each window comprising an initial address and an end address, a match comprising the global address falling between the initial address and the end address (col. 5 lines 10-21).

6. As to claim 18, Brantley, Jr. et al. taught that computing a local address comprised adding an offset of one or more bits to the global address, yielding the local address (fig. 7,

248).

7. As to claim 19, Brantley, Jr. et al. taught computing a local address comprised replacing more or more bits of the global address by a vase value, yielding the local address (fig. 7, 244, 246).

8. As to claim 20, Brantley, Jr. et al. taught that the propagating step comprised propagating the message to a number of processor elements, the number comprising less than all and more than one of the processor elements (fig. 1, col. 8 lines 35-69).

9. As to claims 21-25, they do not teach or define above the invention claimed in claims 16-20 and are therefore rejected under Brantley, Jr. et al. for the same reasons set fourth in the rejection of claims 16-20, supra. As to claim 21's additional limitation of the local data memories of the first and second processing unit not on a common bus, as it clearly seen from figs. 1 and 2, local memory 30 of NODE 0 is not connected to a bus in common with local memory 30 of NODE n, but is instead connected through a network/storage interface unit 28 to a network 10 for communication between nodes as described in the text of the patent.

10. The rejections are respectfully maintained and incorporated by reference as set forth in the last office action, paper number &PPN&, mailed &PPNMD&.

11. New claims 26-29 are rejected under 35 USC 102(b) as being clearly anticipated by Brantley, Jr. et al., U.S. Patent 4,980,822.

As new claim 26 is word for word identical to old claim 16 plus claim 17, new claim 27 is word for word identical to old claim 16 plus claim 20, new claim 28 is word for word identical to old claim 21 plus claim 22, and new claim 29 is word for word identical to old claim 21 plus 25, the rejections of claims 16+17, 16+20, 21+22, and 21+25 equally apply to new claims 26-29 and are herein incorporated by reference to the prior office action, paper number 7, mailed July 3, 2002.

12. New claims 30 and 31 are rejected under 35 USC § 103 as being unpatentable over Brantley, Jr. et al., U.S. patent 4,980,822, in view of Costa et al., U.S. Patent 5,247,673.

13. As to new claims 30 and 31, Brantley, Jr. et al. did not teach the claimed "two address

windows". However, Costa et al. taught two address windows (fig. 4, global shared P-REGION shows three shared address windows SHM). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Costa et al.'s multiple shared address windows with the teachings of Brantley, Jr. et al. because Costa et al. states that having multiple shared address windows provides an advantage in allocating and sharing memory between plural CPU's (col. 3 lines 46-58, col. 4 lines 3-25, col. 7 lines 32-34, and col. 11 lines 14-20).

14. New claim 32 is rejected under 35 USC 102(b) as being clearly anticipated by Shi, U.S. Patent 5,517,656.

Shi taught (e.g. see figs. 6-21) the invention as claimed (as per claim 32), including a data processing ("DP") system comprising:

A) a method of operating a parallel computer system (col. 2 lines 3-5) having at least first, second and third processor elements (fig. 20, "CPU", showing three units), each processor element comprising a processor (col. 3 lines 54-56), a local program memory (col. 3 lines 57-58), a local data memory (col. 3 lines 57-58), a communications manager (fig. 17, 605, 600, 595, 590, 610, 615, 620, 625) and an operating system (fig. 17 585), within each processor element the local program memory, local data memory, and communications manager all communicatively coupled by means of a common bus (by defining the processor elements as conventional computers running conventional operating systems (col. 7 lines 56-61), Shi has inherently indicated that the elements are interconnected by a common bus), the communications managers of the at least first and second processor elements communicatively coupled by means of a message-passing communications network (fig. 17, 120), the processor elements each executing an application (col. 5 lines 19-25), each communications manager further comprising predefined values indicative of global addresses in which the application of the processor element is interested (col. 5 lines 24-41), the method comprising the steps of:

B) writing, by the processor of the first processor element, by means of the common bus of the first processor element, a result of a computation into the communications manager of the first processor element (col. 5 lines 9-13);

C) adding, by the communications manager, a global address to the result of the computation (col. 2 lines 24-30 and col. 4 lines 21-25);

D) propagating, on the message-passing communications network, a message comprising the global address and the result of the computation (col. 2 lines 29-32 and col. 4 lines 21-25);

E) receiving the message, via the message-passing communications network, by the communications manager of the second processor element (col. 5 lines 30-36);

F) comparing, by the communications manager of the second processor element, the global address with the predefined values for a match (col. 14 lines 40-47);

G) achieving a match thereof (col. 14 lines 40-47);

H) computing a local address by the communications manager of the second processor element, and storing the results of the computation at the local address via the common bus to the local data memory (col. 14 lines 37-39);

I) receiving the same message, via the message-passing communications network, by the communications manager of the third processor element (col. 4 lines 30-35, col. 5 lines 12-15);

J) comparing, by the communications manager of the third processor element, the global address with the predefined values for a match (col. 17 lines 11-16);

K) achieving a match thereof (col. 17 lines 11-16); and,

L) computing a local address by the communications manager of the third processor element, and storing the results of the computation at the local address via the common bus to the local data memory (col. 17 lines 11-16).

15. As applicant submitted no arguments in paper number 10, filed November 24, 2002, no response can possibly be provided.

16. **THIS ACTION IS MADE FINAL**. Applicant is reminded of the extension of time policy as set forth in 37 CFR § 1.136(a). The practice of automatically extending the shortened statutory period an additional month upon the filing of a timely first response to a final rejection has been discontinued by the Office. See 1021 TMOG 35.

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 CFR § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

17. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (703) 305-9690. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712. The fax phone numbers for this Group are: After-final: (703) 746-7238; Official: (703) 746-7239; Non-Official/Draft: (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Richard Ellis
February 6, 2003

Richard Ellis
Primary Examiner
Art Unit 2183